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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/159,397	09/23/1998	SAU C. WONG	M-10296 US	5079

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EXAMINER	
WHIPKEY, JASON T	

ART UNIT	PAPER NUMBER
2612	

DATE MAILED: 10/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/159,397	WONG ET AL.	
	Examiner	Art Unit	
	Jason T. Whipkey	2612	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *15 and 24* is/are allowed.

6)☒ Claim(s) *1-14,16-23,25 and 26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 May 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, see pages 8-9, filed June 14, 2004, with respect to the rejections of claims 1-14, 16-23, 25, and 26 under 35 U.S.C. 103 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground of rejection is made.

Claim Rejections - 35 U.S.C. § 103

2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. § 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 C.F.R. § 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. §§ 102(e), (f) or (g) prior art under 35 U.S.C. § 103(a).

4. Claims 1-7, 10, 12, 18-22, and 26 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Kawamura (U.S. Patent No. 5,576,759) in view of Shibata (U.S. Patent No. 6,011,714).

Regarding claims 1 and 18, Kawamura discloses a digital still camera. As shown in Figure 2, the camera includes image processing unit 1 containing a CCD ("an image sensor") that outputs analog signals (column 4, lines 26-32). Captured image signals are processed and compressed in compression and expansion unit 5 ("image processing and compression circuits") (column 5, lines 3-4). Intermediate to image processing unit 1 and compression and expansion unit 5 is main buffer memory 3, which receives and stores one frame of image data and transmits it to compression and expansion unit 5 (column 4, lines 38-40, and column 5, lines 1-4).

Kawamura is silent with regard to main buffer memory 3 being an analog/multi-level memory.

Shibata discloses a memory that is capable of storing analog and multi-valued data, such as an image (column 1, lines 27-32, and column 2, lines 50-54). As stated in column 1, lines 16-26 and 32-37, an advantage to using an analog or multi-valued memory in place of a traditional digital memory is that a larger quantity of data may be stored with less processing. For this reason, it would have been obvious at the time of invention to have Kawamura's digital still camera include an analog or multi-level memory.

Shibata is silent with regard to including a memory that is "high density" (a relative term that the Applicant does not define).

Official Notice is taken that memory can be produced in varying capacities by combining virtually any number of memory elements into a single package, the sizes of which are becoming increasingly miniscule.

An advantage to using a "high density" memory is that a large amount of data may be stored without greatly increasing the overall size of the apparatus. For this reason, it would have been obvious to one of ordinary skill in the art for Shibata to maximize memory capacity while minimizing the size of that memory.

Regarding claims 2 and 20, both Kawamura and Shibata are silent with regard to the exact size of their respective memories.

The courts have held that "where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955).

While Shibata does not specifically teach that the analog/multi-valued memory can receive data "at a rate of greater than 10 Mbits/sec for more than 5 seconds and stored more than 50 Mbits of said data", it would have been *prima facie* obvious at the time of invention to do so, as Applicant merely found the optimum memory parameters for use with the imaging device described by Kawamura.

Regarding claim 3, Kawamura teaches that image processing unit 1, which includes the CCD, outputs analog image signals (column 4, lines 30-32).

Regarding claim 4, Shibata is silent with regard to converting image signals stored in analog form to digital form before processing.

Official Notice is taken that image signals are commonly converted to digital form before image processing occurs. An advantage to performing image processing on digital signals is that digital processing components are much more inexpensive than analog processing components. For this reason, it would have been obvious at the time of invention to have Shibata's memory convert the stored signals to digital form for processing.

Regarding claim 5, Kawamura teaches that captured image signals are compressed in compression and expansion unit 5 ("image processing and compression circuits") (column 5, lines 3-4).

As for claims 6 and 21, Kawamura teaches that the control unit 8 controls the circuitry of the camera. It is inherent that memory 3 transfers data to compression and expansion unit 5 when it is available for processing; otherwise, compression could not occur and the system would be inoperable.

Regarding claims 7 and 22, Kawamura teaches that his device is a digital still camera (column 1, line 10).

Regarding claims 10 and 12, Kawamura teaches that Figure 2 shows the circuitry employed in a digital still camera (column 4, lines 21-23).

Regarding claim 19, Kawamura teaches that image processing unit 1 performs signal processing on the image signals before they are stored in memory 3 (column 4, lines 30-32).

Regarding claim 26, Kawamura teaches that the image data is stored in memory 3 before transmission to compression and expansion unit 5 (column 5, lines 1-4).

5. Claims 8, 9, and 25 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Kawamura in view of Shibata and further in view of Fernandez (U.S. Patent No. 5,644,636).

Claims 8 and 25 may be treated like claims 7 and 1, respectively. However, both Kawamura and Shibata are silent with regard to having the analog memory contained in a removable memory card.

Fernandez shows in Figure 2 an EEPROM 50. The EEPROM may be included as part of a removable card, such as a bankcard for an automated teller machine (column 5, lines 14-17). The EEPROM may be written to with write commands (column 5, lines 39-40). The EEPROM memorizes a level of signal charge in its memory cells (column 4, lines 54-59), making it an analog memory. The memory may be read via lines 60 and 62.

The advantage to using a removable analog memory is that many analog memories may be used with one recording device, which increases the amount of data that can be stored using one recording device. For this reason, it would have been obvious to have Kawamura's camera include a removable analog memory card.

Regarding claim 9, Fernandez teaches that an analog-to-digital converter 46 may be included on a card with EEPROM 50 (column 5, lines 17-19). The advantage of including an A/D converter on a removable card is that it allows a system that processes digital data to use analog data stored on the card. For this reason, it would have been obvious to have Kawamura's camera include an A/D converter on a removable memory card.

6. Claim 11 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Kawamura in view of Shibata and further in view of Anderson (U.S. Patent No. 6,177,956).

This claim may be treated like claim 7. However, both Ohmi and Roberts are silent with regard to placing the image processing and compression circuits outside the camera.

Anderson discloses an imaging device 14 and a computer 18 connected by a bus 16. Computer 18 may be separate imaging device 14 (column 3, lines 49-51). The computer performs image processing and compression on the raw image data received from the camera (column 12, lines 9-11, 15-16, 26-29, and 48-50). An advantage to having an external device perform image processing and compression is that the external device may have more space for processing circuitry, which decreases the power used by, and the size of, the digital camera. For this reason, it would have been obvious to have Kawamura's imaging system perform image processing and compression outside the camera.

7. Claims 13, 14, and 16 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Kawamura in view of Shibata and further in view of Simko (U.S. Patent No. 4,989,179).

Regarding claims 13 and 16, Simko discloses an analog signal recording and playback system that includes array 13 with a plurality of columns that act as write pipelines, wherein each column includes multiple non-volatile memory cells (column 3, lines 58-60). Each column includes a write column driver 15 to write data to the cells (column 3, lines 64-66). Cells are programmed using a voltage provided by high voltage source 150, which is shown in Figure 5, to produce a charge in the selected cell (column 10, lines 45-56). The cells may record data using multi-level storage (column 12, lines 43-46). Each column of cells in the array (Figure 3) is used to store data independently (column 5, lines 38-41).

Clock addressing sequencer 22 acts as a timing circuit (column 4, lines 14-30) to drive column drivers 15 sequentially (column 3, lines 64-66). A high voltage source at terminal 150 (Figure 5) provides a programming voltage. The programming voltage is applied incrementally, and comparator 66 (Figure 3) compares the voltage in the cell with the expected voltage after each increment (column 11, lines 35-56) to verify the contents of the cell.

Official Notice is taken that charge pumps are a common way to produce a voltage higher than a provided supply voltage. Since Simko is silent with regard to how this high voltage is produced, it would have been obvious to use any high voltage generator suitable for programming memory cells, such as a charge pump.

As stated in column 2, lines 17-21, an advantage to using such a memory is that data can be stored in less space. For this reason, it would have been obvious at the time of invention to have Kawamura's camera include Simko's memory.

Regarding claim 14, Simko teaches that the memory cells included in his system can store analog information (column 2, lines 43-46).

8. Claim 17 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Kawamura in view of Shibata and further in view of Simko and Chen (U.S. Patent No. 5,867,430).

Claim 17 may be treated like claim 16. However, Simko is silent with regard to using two banks and performing a verification cycle on one while performing a programming operation on the other.

Chen discloses a flash memory device with two banks (Figure 1). Bank 0 and bank 1 are arrays of non-volatile memory cells (column 3, lines 33-35). As one bank is being programmed, the other bank may be read and verified using verify sense amplifier 176 (column 5, lines 38-44).

An advantage to performing simultaneous verification and writing on two banks is that accurate data may be stored at a faster speed than in the case where such operations are performed sequentially. For this reason, it would have been obvious at the time of invention to have Simko's storage system perform simultaneous writing and verification using two banks of memory cells.

9. Claim 23 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Kawamura in view of Shibata and further in view in view of Wright (U.S. Patent No. 6,172,935).

Claim 23 may be treated like claim 18. However, Kawamura is silent with regard to the structure of the memory device used.

Wright discloses a memory device 200 (Figure 3) comprised of memory banks 211A and 211B, each including a plurality of memory cells (column 9, lines 49-55). The system uses charge pump voltage Vccp to select the row to be read (column 64, lines 3-13). A charge is then applied to the cell to produce a certain voltage (column 72, lines 43-47).

When writing data, bits may be alternately programmed into banks 211A and 211B (column 22, lines 35-39). For example, if a first bit is written into bank 211A, a second bit is written into bank 211B, and a third bit is written into 211A, then programming of bank 211B begins after the programming of bank 211A has begun but before it is complete (since the third bit has not yet been written).

An advantage to using a memory system with multiple banks is that both banks may be simultaneously operative, which speeds up storage and retrieval times. For this reason, it would have been obvious at the time of invention to have Kawamura include a dual-banked memory system like the one described by Wright.

Allowable Subject Matter

10. Claims 15 and 24 are allowed.

No prior art could be located that teaches or fairly suggests an analog/multi-level memory with a plurality of odd- and even-numbered pipelines that perform simultaneous programming and each using one of two voltages.

Conclusion

11. This action is non-final because a new ground of rejection is being applied to claims that are unamended.

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason T. Whipkey, whose telephone number is (703) 305-1819.

The examiner can normally be reached Monday through Friday from 8:30 A.M. to 6:00 P.M. eastern standard time, alternating Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wendy R. Garber, can be reached on (703) 305-4929. The fax phone number for the organization where this application is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application should be directed to the Technology Center 2600 Customer Service Office, whose telephone number is (703) 306-0377.

JTW

JTW
October 1, 2004

WENDY R. GARBER
SUPERVISORY PATENT EXAMINER
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